Distributed modeling of 4-port transistor for linear mmW design application

Wafa Khelifi*, Tibault Reveyrand*, Julien Lintignat*, Bernard Jarry*, Raymond Quéré*, Luc Lapierre†,
Vincent Armengaud†

*XLIM, 123 av. Albert Thomas, 87060 Limoges Cedex, France
†CNES, 18 av. E. Belin, 31400 Toulouse, France

Abstract—**This paper presents an approach for the distributed modeling of a 4-port transistor. The proposed principle relies on considering any multi-finger transistor as the association of a number of elementary active linked together with extrinsic passive networks. An electromagnetic analysis allows to set the electrical equivalent scheme of the passive networks whereas the internal active device is defined by an equivalent model. It is shown how the equivalent intrinsic device (based on 2 fingers) and the values of the suitably defined distributed parasitic network elements can be accurately extracted and modeled on the basis of standard measurements. This approach is validated by the comparison of measured and simulated results for a GaAs HEMT transistor in the Ku-band.**

Index Terms—**Electromagnetic analysis, GaAs HEMT, S-parameters, characterization, modeling.**

I. INTRODUCTION

The development of high-performance microwave and MMIC circuits requires accurate computer aided design (CAD) tools in the design phase [1]. Indeed, the success of the design usually relies on the quality of non-linear transistor model. In this context, accurate electrical device model that describes the operation up to millimeter-wave frequencies is a key aspect.

Conventional scalable models, provided within Process Design Kits (PDKs), are based on equivalent circuits whose parameters are scaled with device size and finger number [2]. Some of these approaches may not be sufficient when operating at high frequencies. Indeed, a large number of measurements must be made on different device structures in order to obtain a good evolutionary model. However, special attention to extrinsic networks modeling and identification should be given.

Furthermore, the distributed effects, which occurs at very high frequencies, can greatly reduce the performance of the transistor. Such behavior is not easy to identify by a simple extrinsic network [3]. Distributed effects must be taken into account in the modeling phase of the device or even more complicated equivalent circuit structures must be evaluated [4]. For this problem, some distributed and semi-distributed models have been proposed. Those models are based on electromagnetic simulations (EM) and S-parameters measurements [5], [6]. Although this model is capable of accurate small-signal prediction in 2-ports, it does not present any information on the performance of the transistor when it is used in 3 or 4-ports configuration. The novelty of this work lies in the development

of a 4-ports distributed model. Indeed, the accuracy of this model is illustrated for different transistor configurations:

- 3-ports model with open on one of the source port ;
- 2-ports with two VIA (2 source port are shorted with VIA holes) ;
- 2-ports featuring with unique VIA (one source port is in open and the other one is shorted).

The presented modeling approach has been validated up to 40 GHz for GaAs HEMT from UMS foundry. The accuracy of this approach is highlighted by simulation and measurements comparisons.

II. PRINCIPLE OF MODELING

The proposed approach is based on the partition of the device geometry into a convenient number of elementary intrinsic model (IM) placed along the layout fingers. The intrinsic model is connected to a parasitic structure that is repartitioned between extrinsic (gate, drain, source) elements and interconnection between two intrinsic models (see figure 1). It should be noted that each part of the parasitics network has been simulated in EM. An equivalent network with lumped elements is then set, the values of the elements are initialized thanks to EM simulation and optimized to fit the 4-port measurement results.
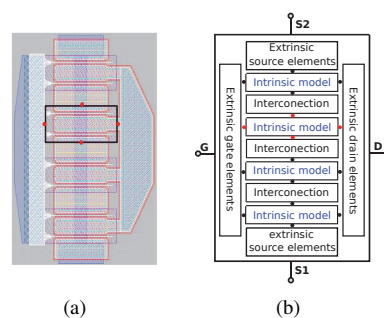

Fig. 1. (a) Transistor layout example. An intrinsic model cell is highlighted. (b) Partitioning of the HEMT transistor. All passive structures are extracted from EM simulation.

The active region of the transistor in figure 1 is partitioned according to the number of gate fingers. The elementary active cell is a two gate fingers-one drain transistor described with an intrinsic 4-ports model (see figure 2). Note that Lg, Rg, Cg, Rd and Ld represent the parasitics effects introduced by the two gate fingers and the drain finger.

The final model topology consists in the embedding of the active elementary cells in the suitably defined passive network. The values of the model elements are then optimized to fit 4-port S-parameters and I-V measurements.
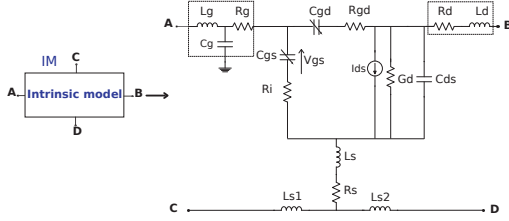

Fig. 2. Electrical circuit of the 4-port intrinsic model cell.

III. MEASUREMENTS

The S-parameters were measured for each point of the I-V network with a Keysight PNA-X vector network analyzer (VNA) on a probe station from 6 GHz to 40 GHz (figure 3). The test fixture used to characterize the transistor is defined by
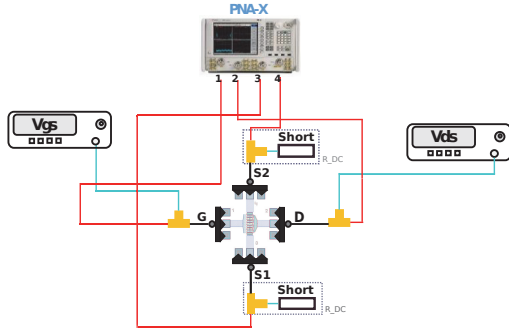

Fig. 3. 4-ports S-parameters and I-V measurements bench.

140 μm interconnection lines with a characteristic impedance of 50 Ω. The dimensions of the probe pads are 88 μm $\times$ 88 μm, and the structures have been laid out for 125 μm-pitch probes. It is worth-noting that for the RF measurements, a de-embedding has been applied in addition to the calibration in order to remove the effects introduced by these interconnection lines [7]. The 4-ports transistor characterization is performed with a short applied to DC. Since this short is non-ideal, its DC resistance value, seen in the source reference plane, is properly identified. Its value will be obtained during the DC model extraction of the transistor. In order to ensure the stability of the transistor, a resistance of 50 Ω has been connected to the RF ports of the bias tee.

IV. NON-LINEAR DEVICE MODELING

The non-linear current source for each intrinsic 4-ports model is based on the modified Tajima equations [8]. Figure 4 shows the DC measurement and simulation results of a 8*60 μm GaAs HEMT in 4-port configuration. Moreover, the parasitic resistive value applied to the shorted source access is taken into account during the DC parameters extraction values of the transistor. As it can be seen, the predicted DC

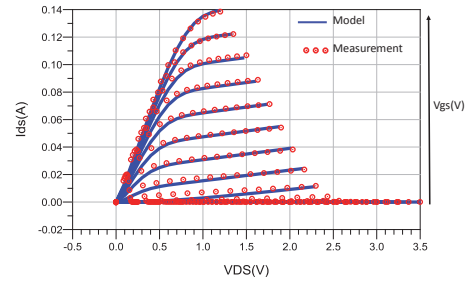curves for the scaled devices are in excellent agreement with measurements.

Fig. 4. Comparison between the I-V measured and simulated curves of a 8*60 μm GaAs HEMT (Vgs is stepped from -1.5 V to +0.2 V with a step of +0.1 V).

V. VALIDATION OF THE PROPOSED MODEL

A. S-parameters validation

In order to validate the proposed transistor model, the measured and the simulated S-parameters have been compared. Note that the S-parameters measurement set up presented on figure 3 is kept, i.e. the DC on the two source pin is shorted and the RF is connected to a 50 Ω resistance. Figure 5 illustrates a comparison between the measured S-parameters and the simulation of the developed model for several bias points. It can be observed that the simulated and measured S-parameters of the transistor are in quite good accordance for a frequency band of 6 GHz up to 40 GHz.
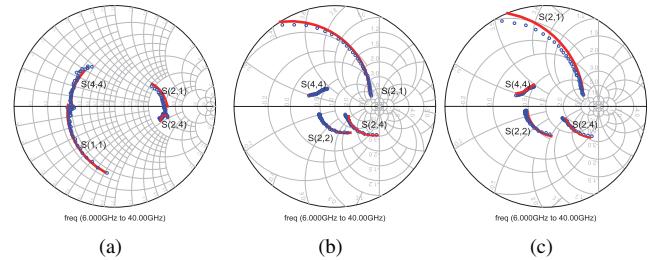

Fig. 5. Comparison between S-parameters measurement (blue symbols) and proposed model simulation (red) for a 8*60 μm GaAs HEMT at Vds=0 V, Ids=0 mA (a); Vds=2 V, Ids=23 mA (b) and Vds=1 V, Ids=119 mA (c).

B. Model validation in different configurations

In addition to this validation, the 8*60 μm GaAs HEMT transistor is analyzed for different topology configurations (see figure 6).

1) 3-port configuration with open on one source port:
In the first structure, the measured transistor has one source port in open circuit (figure 6-1). As this open is not ideal, in the distributed model simulation, we have identified its capacitance equivalent model, whose value is optimized, in order to ensure a consistency between measurements and simulations of the S-parameters where all the parameters of model are kept constant. S-parameters, plotted in figure 7, validate the topology of our 4-port distributed model in this configuration.
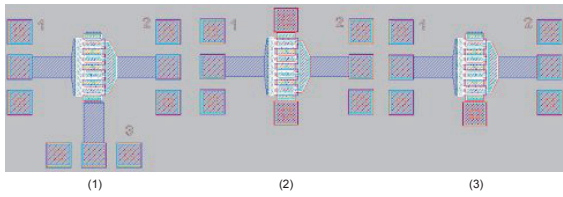
Fig. 6. Layout plan figures of the test structures used to analysis different topology.
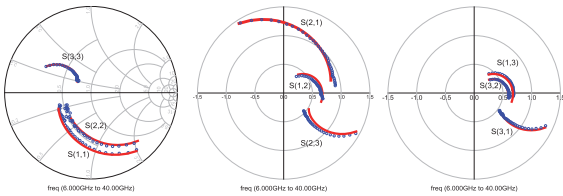

Fig. 7. Comparison between S-parameters measurement (blue) and model simulation (red) for a 8*60 μm GaAs HEMT at (Vds=2 V, Ids=23 mA) on the 3-port structure illustrated on fig. 6-1.

2) Standard 2-ports configuration:

In this section, a 2-port transistor with the same dimensions but where each source pin is connected to VIA holes (figure 6-2) is measured. In the same time, in the distributed model simulation test bench, VIA are connected to both source pin. Simulations and measurements results are compared in figure 8.
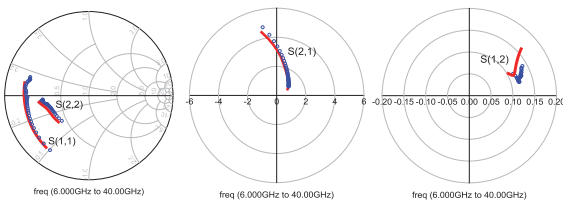

Fig. 8. Comparison between S-parameters measurement (blue) and model simulation (red) for a 8*60 μm GaAs HEMT at (Vds=2 V, Ids=23 mA) on the standard 2-port structure illustrated on fig. 6-2.

The I-V network measurements of the conventional transistor configuration and the distributed model in 2-ports are depicted in figure 9 in order to verify the accuracy of the non linear model.
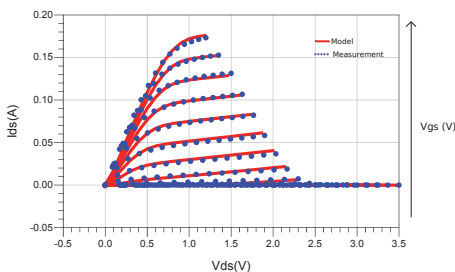

Fig. 9. Comparison between the I-V measured and simulated curves of a 8*60 μm GaAs HEMT (Vgs is stepped from -1.5 V to +0.2 V with a step of +0.1 V).

3) 2-ports configuration with a single VIA:

In the last structure, the measured transistor has a unique VIA hole, the other source connection is left open (figure 6-3). On the other hand, one source pin of the distributed model is connected to the VIA hole model and the other one is connected to the capacitance modeling the open access. Figure 10 illustrates a comparison between simulations and measurements S-parameters. The results of the developed model are shown to be in satisfactory agreement with the measurements over the whole 6-40 GHz.
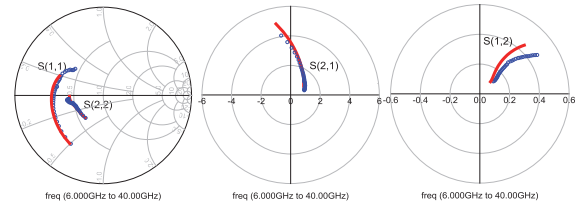

Fig. 10. Comparison between S-parameters measurement (blue) and model simulation (red) for a 8*60 μm GaAs HEMT at (Vds=2 V, Ids=23 mA) on the 2-port structure using a single VIA hole illustrated on fig. 6-3.

VI. CONCLUSION

In this paper, a 4-port distributed model of a 8*60 μm GaAs HEMT transistor has been proposed. The modeling approach enables to determine a multi-bias model on the basis of electromagnetic simulations of the parasitics network layout, S-parameters and I-V network measurements. This new model presents a good accuracy which has been validated through DC and RF measurement results for different layout configurations.

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