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Experimental study on effect of second-harmonic injection at input of classes F and F^{-1} GaN power amplifiers

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This presented study focuses on the impact of gate-source voltage waveforms on power added efficiency performances of GaN HEMTs for the design of class F and class F^{-1} amplifiers. It is shown that second-harmonic signal injection at the gate port of transistors can lead to efficiency improvements in the case of class F operation and efficiency deteriorations in the case of class F^{-1} operation. This work is applied to a 15 W GaN HEMT die from Cree at a fundamental frequency Fo equal to 2 GHz. Calibrated on-wafer time domain measurements are reported.

Introduction: AlGaN/GaN HEMT technology offers good potentialities for high-efficiency high power microwave amplification because of high current densities and high breakdown voltage. High efficiency performances of microwave power amplifiers are reached when fundamental and harmonic frequency components (Fo, 2Fo, 3Fo) are terminated into appropriate impedances. High efficiency harmonic tuned microwave power amplifiers have been widely reported during the past few years [1–6].

In this Letter, we focus on class F and class F^{-1} operation modes and examine a possible way to increase efficiency performances using active second-harmonic signal injection at the gate port of GaN HEMTs. An appropriate control of both first and second harmonics of the gate-source voltage results in a quasi-half sine wave shape having a DC level close to or a little above the pinch off voltage of the transistor. Such a gate-source voltage shape results in an aperture time reduction of the drain-source current. Consequently a decrease of the DC drain current and an improvement of efficiency can be obtained. In the following, we demonstrate by experimentation that this technique can be successfully applied to class F amplifiers but is not compliant with class F^{-1} amplifiers.

Second-harmonic injection at input of class F and class F^{-1} GaN amplifiers: On-wafer calibrated time domain waveform measurements of a 15 W GaN HEMT die from Cree have been performed using a test bench shown in Fig. 1. Two synchronised generators (respectively at frequencies Fo = 2 GHz and 2Fo = 4 GHz) are used to drive the transistor input. A harmonic tuner (at Fo, 2Fo, 3Fo) is used to set appropriate load terminations of the transistor. A large signal network analyser (LSNA) based on the harmonic sub-sampling technique enables simultaneous measurements of voltage and current waveforms at the gate and the drain ports [7]. Calibrated measurements at the probe tips are then de-embedded to obtain voltage and current waveforms as close as possible to the intrinsic ports of the transistor (see Fig. 1).

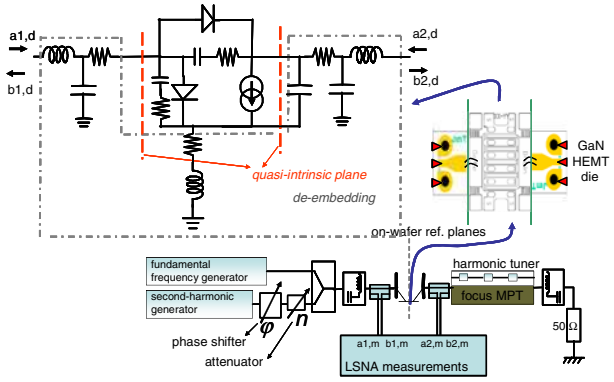

Fig. 1 *Time domain waveform measurement setup*

For class F operation, harmonic load impedances are tuned to: $Z_{L1} = 37 - j2\ \Omega$ at Fo; a low impedance Z_{L2} close to a short at 2Fo and a high impedance Z_{L3} close to an open at 3Fo. For class F^{-1} operation, harmonic load impedances are tuned to: $Z_{L1} = 36.5 - j3\ \Omega$ at Fo; Z_{L2} = open and Z_{L3} = short. In regard to input signal driving conditions, three significantly different measurement scenarios have been performed. First, the input generator at 2Fo is turned off. Source impedance Z_{S2} at 2Fo is equal to 50 Ω. Secondly, the input generator at 2Fo is turned on. Signal injection at the gate port at 2Fo is tuned in magnitude and phase relative to signal injection at the gate port at Fo in order to synthesise Z_{S2} equal to a short. Thirdly, active signal injection at the gate port at 2Fo is tuned in magnitude and phase to reach maximum power added efficiency (PAE).

PAE measurements against output power for class F and class F^{-1} conditions are plotted in Figs. 2*a* and *b*. Measured time domain voltage and current waveforms at maximum PAE performances are plotted in Figs. 3*a–c*. DC drain current I_{ds0}, and drain current component at the fundamental frequency I_{ds1} are plotted against input power in Figs. 4*a* and *b*. Drain-source voltage component V_{ds1} at the fundamental frequency is plotted against input power in Figs. 5*a* and *b*.

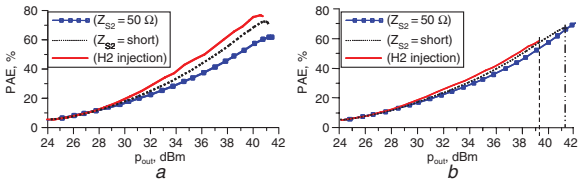

Fig. 2 *PAE against output power*

a Class F operation
b Class F^{-1} operation

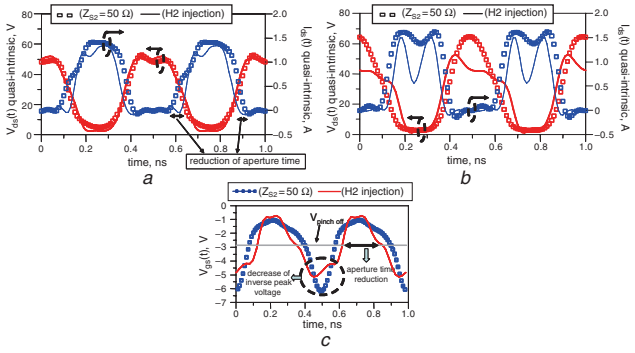

Fig. 3 *Time domain waveform measurements at maximum PAE*

a Drain voltage and current for class F operation
b Drain voltage and current for class F^{-1} operation
c Gate-source voltage for both class F and F^{-1} conditions

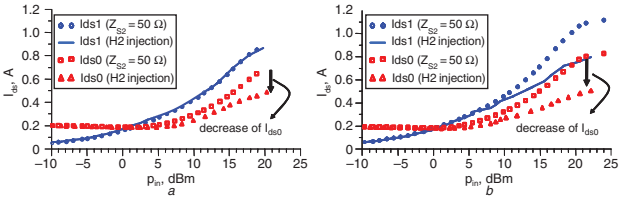

Fig. 4 *Drain current (DC and fundamental components) against input power*

a Class F
b Class F^{-1}

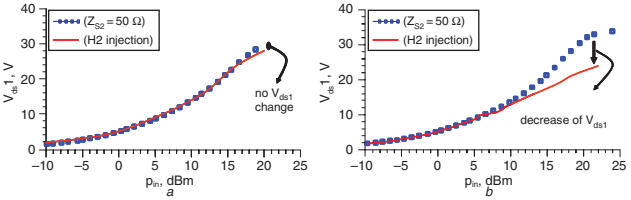

Fig. 5 *Drain voltage (fundamental component) against input power*

a Class F
b Class F^{-1}

Measurement result analysis: For class F operation, appropriate second-harmonic input injection enables obtaining the best performances. 76% PAE and 40.5 dBm output power are reached when the gate-source

voltage waveform has a quasi-half sine shape. When the source impedance at second-harmonic Z_{S2} is a short or a 50 Ω it can be observed in Fig. 2*a* that PAE decreases respectively down to 71 and 60%. The examination of time domain waveforms plotted in Fig. 3*a* clearly demonstrates the benefit of second-harmonic input injection on PAE performances. It can be observed that the aperture time of the drain current is reduced when gate-source voltage shape becomes a quasi-half sine (Fig. 3*c*). Consequently, the DC drain current decreases as indicated by curves plotted in Fig. 4*a*. Another key point is that for class F operation load impedance at 2Fo is a short circuit. In the presence of a significant gate-source voltage component at 2Fo, the voltage controlled drain-current source of the transistor generates an additional quantity of drain current at 2Fo which is terminated into a short. Therefore, drain-source voltage conditions of the transistor are not significantly modified, and the resulting drain voltage component at the fundamental frequency do not vary, as can be observed in Fig. 5*a*. For all the reasons mentioned above, PAE performances are improved in the case of second-harmonic injection at the gate port with a level 10 dB lower compared to the fundamental component level. Furthermore, in that particular case, the negative peak of the gate-source voltage is reduced (see Fig. 3*c*). This can be favourable considering reliability aspects of the device.

Class F^{-1} operation: For class F^{-1} operation, second-harmonic injection deteriorates PAE performances, as can be seen in Fig. 2*b*, despite the fact that I_{ds0} decreases (Fig. 4*b*) for the reasons previously explained. The main reason is because for class F^{-1} operation Z_{L2} is a high impedance (close to an open).

In the presence of a significant gate-source voltage component at 2Fo, the voltage controlled drain-current source of the transistor generates an additional quantity of drain current at 2Fo which is antagonist with high impedance load conditions at 2Fo. Therefore, drain-source voltage conditions of the transistor are significantly modified, as can be observed in Fig. 3*b*, and the resulting V_{ds1} decreases (see Fig. 5*b*). As a consequence, the saturated output power decreases and is reached at a lower input power, as it can be observed in Fig. 2*b*. Both output power and PAE performances are deteriorated.

Conclusion: Calibrated on-wafer time domain measurements have demonstrated PAE improvement or degradation owing to second-harmonic manipulation at the gate port of GaN HEMTs. The analysis of voltage and current waveforms have demonstrated that second-harmonic injection at the gate port of the transistor can lead to PAE improvement provided that load impedance at the second harmonic is a low impedance. This work provides useful information to aid in designing high efficiency multi-stage harmonic tuned power amplifiers. For example, study of cascaded class F^{-1} and class F circuit topologies can be investigated.

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One or more of the Figures in this Letter are available in colour online.

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References

1 Grebennikov, A., and Sokal, N.O.: 'Switchmode RF power amplifiers', (Newnes, Oxford, 2007)
2 Woo, Y.Y., Yang, Y., and Kim, B.: 'Analysis and experiments for high-efficiency class-F and inverse class-F power amplifiers', *IEEE Trans. Microw. Theory Tech.*, 2006, **54**, (5), pp. 1969–1974
3 Wright, P., Lees, J., Tasker, P.J., Benedikt, J., and Cripps, S.C.: 'An efficient, linear, broadband class-J-mode PA realised using RF waveform engineering'. Int. Microwave Symp., Boston, MA, USA, June 2009, paper WE2E-5
4 White, P.: 'Effect of input harmonic terminations on high efficiency class B and class F operation of PHEMT devices,' in IEEE MTT-S Int. Symp. Dig., Baltimore, MD, USA, June 7–12, 1998, Vol. 3, pp. 1611–1614
5 Colantonio, P., Giannini, F., Giofre, R., Limiti, E., Serino, A., Peroni, M., Romanini, P., and Proietti, C.: 'A C-band high-efficiency second-harmonic-tuned hybrid power amplifier in GaN technology', *IEEE Trans. Microw. Theory Tech.*, 2006, **54**, (6), pp. 2713–2722
6 Gao, S., Butterworth, P., Ooi, S., and Sambell, A.: 'High-efficiency power amplifier design including input harmonic termination', *IEEE Trans. Microw. Wirel. Compon. Lett.*, 2005, **16**, (2), pp. 81–83
7 Reveyrand, T., Mallet, A., Nébus, J.M., and Vanden Bossche, M.: 'Calibrated measurements of waveforms at internal nodes of MMICs with a LSNA and high impedance probes'. 62nd ARFTG Conf. Dig., pp. 71–76, Boulder, CO, USA, December 2003