GaN transistor characterization and modeling activities performed within the frame of the KorriGaN project

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The present paper presents the transistor modeling work achieved in the GaN European project KorriGaN ("Key Organisation for Research in Integrated Circuits in GaN technology"). The KorriGaN project (2005–09) has released 29 GaN circuits such as high-power amplifiers (HPAs), low-noise amplifiers (LNAs), and switches. Modeling is one of the main key to reach successful designs. Therefore, nonlinear models of European GaN HEMT models have been developed. This work deals with characterization tools such as pulsed IV, pulsed [S] parameters, load-pull measurements, and measurement-based methods to perform GaN HEMT compact models parameters extraction. The present paper will describe the transistor modeling activities in KorriGaN for HPA designs (nonlinear models including trapping and/or self-heating effects) and LNA designs (nonlinear models and noise parameters).

I. INTRODUCTION

KorriGaN has been the largest project about GaN technology. It was launched by EDA (European Defense Agency) in 2005 [1] for a total duration of 54 months. The main purposes of this project were:

– to establish a complete and independent European chain in GaN technology from wafer to the final transreceiver Module for Radar applications;
– to demonstrate the performances and the reliability at sub-system level of this GaN technology for defence applications.

Seven countries were involved in this huge project: France, Germany, Italy, Netherlands, Spain, Sweden and the United Kingdom. KorriGaN was splitted into six sub-projects: systems specifications, materials (wafers and epitaxies), foundry works (including the modeling aspect of the transistors), reliability, thermal integration, and final demonstrators. Several functionalities, for which GaN technology is very promising, have been designed: S, X, and broadband (2-6, 2-18) high-power amplifiers (HPAs); X band and broadband robust low-noise amplifiers (LNAs); and switches.

Four foundries were involved in the project : 3-5 Lab (F), Chalmers (Sw), QinetiQ (UK) and Selex-SI (I). Twelve designers teams worked with those foundries : 3-5 Lab (F), BAE Systems Insyte (UK), Indra (Sp), Isom (Sp), Eletronica (I), Saab (Sw), Selex SAS (UK), Selex SI (I), Thales Defence Ltd. (UK), TNO (NL) and UMS (G).

The measurement-based compact modeling activity (Workpackage WP3.3) was the interface between foundries and designers. Four labs have released transistor models for designers: Chalmers, Politecnico di Torino, University of Roma Tor Vergata and XLIM.

The KorriGaN project has released up to 29 demonstrators in different technologies (coplanar and microstrip) in two runs. The modeling part was essential in the design process of all those demonstrators.

The present paper will describe the workpackage dedicated to measurement-based modeling into the KorriGaN project as well as the main results achieved in the framework of this project. Detailed results about the various advances made in the project have been given elsewhere.

First of all, an overview of the characterization and modeling activities in KorriGaN, will be presented, then the different measurements setups. A part will be dedicated to an example of nonlinear modeling from the device to the final demonstrator. Finally, some research activities about self-heating, trapping effects, and noise modeling will be presented.

II. KORRIGAN MODELING WORKPACKAGE ACTIVITY

The modeling activities took place during 36 months. This workpackage (named WP3.3) was in charge of the characterization

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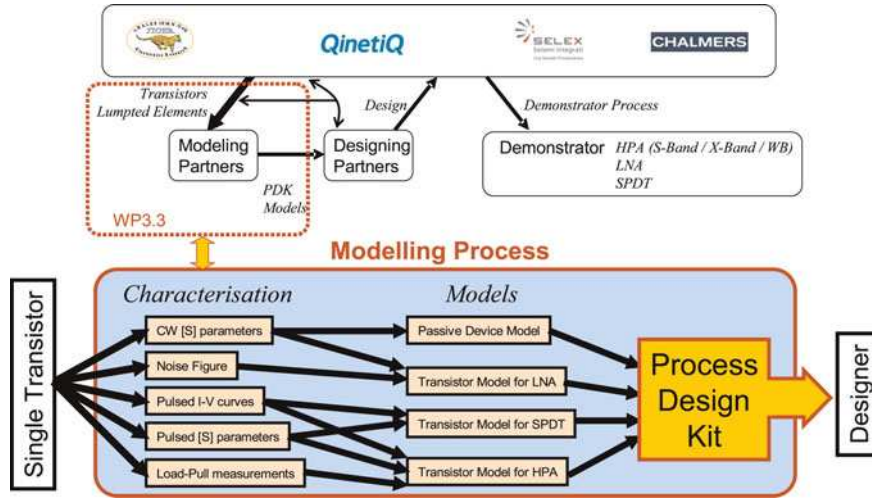T. Reveyrand
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Fig. 1. KorriGaN Modeling Workpackage (WP3.3) activity organization.

and the modeling of both passive (capacitors, resistors, etc.) and active (transistors) devices. This work leads to the creation of a complete PDK (Process Design Kit) and of a design guide for each foundry (Chalmers, QinetiQ, Selex-SI and Tiger).

The characterization and modeling of passive devices are based on classical [S] parameters measurements up to 40 GHz.

Regarding the active devices, several measurement methods has been used such as CW and pulsed [S] parameters measurements, DC and pulsed I–V characterizations, large-signal measurements (load-pull), and noise measurements.

The released transistor models depend on the final application: noise models for LNAs, linear models for switches, nonlinear models for HPAs and LNAs, electro-thermal models, and trapping effect models for some HPAs.

Figure 1 illustrates where the WP3.3 work package is located into the global KorriGaN project.

III. MEASUREMENT SETUPS

The first step for the HEMT compact modeling is the characterization of a representative transistor. For this purpose, several measurement setups are used such as [S] parameters, pulsed IV and pulsed [S] parameters, and noise parameters

for model extraction and load-pull setup for large-signal verification of nonlinear models.

A) S parameters

CW [S] parameter measurements have been performed by foundries for testing and selecting devices on a complete wafer and by modeling partners who can extract a linear model, a table model, or the noise parameters from such measurements.

Regarding the foundries activities, the main test is to map where are the transistors on the completed wafer with typical h21, Gmax, and Ft values.

B) Pulsed measurements

The pulsed [S] parameters measurement setup is useful to extract nonlinear elements dependencies in a nonlinear model [2]. The bench used at XLIM enable pulsed IV and [S] parameters measurements into a 500 ns pulse with a 10-µs period as illustrated in Fig. 2.

This setup is based on the use of Agilent 8110A and 8115A pulse generators. Those generators are limited to 100 V/2 A on a 50 Ω loadline (i.e. 100 V with no current or 2 A with no
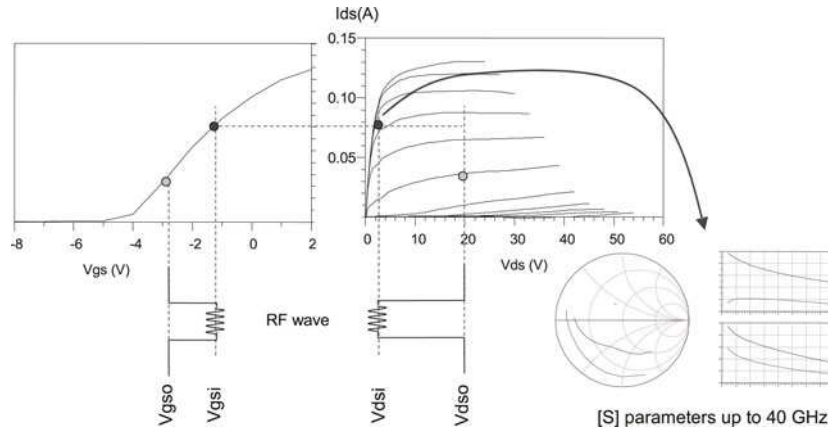

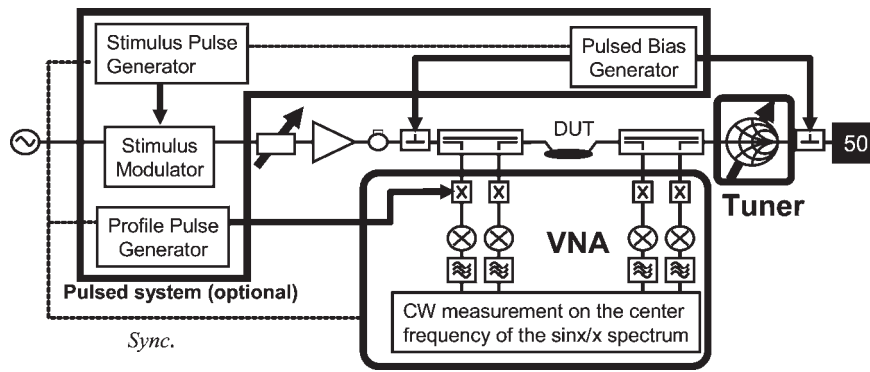**Fig. 2.** Pulsed IV and [S] parameters measurement principle.

Fig. 3. (Pulsed) Frequency domain passive load-pull at XLIM.

voltage). This bench was sufficient for the elementary transistors characterized in the KorriGaN project but is not sufficient for larger transistors such as commercially available packaged GaN transistors from Japan or the USA and thus the upcoming large periphery packaged transistors from Europe. New pulsed IV solutions appeared recently for that purpose like the PIV system by AMCAD Engineering which enable 240 V and 10 A simultaneously.

The modeling of a transistor requires a network with a bias quiescent bias point established by the designer of the final application and which corresponds to the bias of the transistor in the real conditions. For each instantaneous bias of the network, [S] parameters are measured up to 40 GHz. Therefore, it is possible to extract a linear model for each measured point and then comes the variations of the nonlinear elements to build the nonlinear model.

C) Load-pull measurements

The load-pull measurement setup is the "Large-Signal" characterization tool used to validate a model or to check the possibilities of a given transistor in terms of output power or power-added efficiency.

The principle of the load-pull setup is to measure the signals at the input and the output of the transistor when moving the load-impedance. There were two methods to modify the load-impedance in KorriGaN: an active and a passive system (Fig. 3).

The active system principle relies on applying an RF signal at the output of the transistor. This signal is synchronized with the one generated by the transistor. Thus, loading conditions at the output of the device under test are artificially created.

The passive system is based on the use of an automated mechanical tuner. The tuner is a line with a mobile resonator (stub). Moving the stub during the measurements enables to map the complete smith chart at the desired frequency.

Load-pull measurements are done on every transistor to validate the model extracted from IV and [S] parameters, in large-signal conditions.

IV. NONLINEAR MODEL FOR HPA

Figure 4 illustrates a classical nonlinear model (no thermal and no trapping effect) released in the frame of KorriGaN. This model has been implemented in ADS software as Software Defined Device (SDD). First of all, a linear model

is extracted from a CW [S] parameters measurement. Then nonlinear elements dependencies are fitted according to pulsed IV and pulsed [S] parameter measurements (a complete pulsed network with a quiescent bias point given for the transistor's final application). The model is then validated thanks to large-signal measurements (load-pull), as illustrated in Fig. 5.

For HPAs, nonlinear models include electro-thermal effects (for large periphery) and trapping effects (if needed) have been released. Those two main parasitic effects have been analyzed during the KorriGaN project and modeling teams has released a new kind of model that take into account those phenomenon.

A complete process from materials to the measured X-band HPA in the frame of KorriGaN has been given with details in [3]. The amplifier is a two-stage amplifier. The first stage is composed of two 12×100 μm transistors and the second stage of four 16×140 μm (Fig. 6). In this case, the foundry was Tiger/3-5 Labs, the design kit has been released by XLIM from the modeling workpackage and the designers are from 3-5 Labs. The result is a 58 W, 38% PAE MMIC amplifier at X-Band.

V. ELECTRO-THERMAL MODELING

The development of accurate device models for GaN-based high-power amplifiers requires to allow for a description of
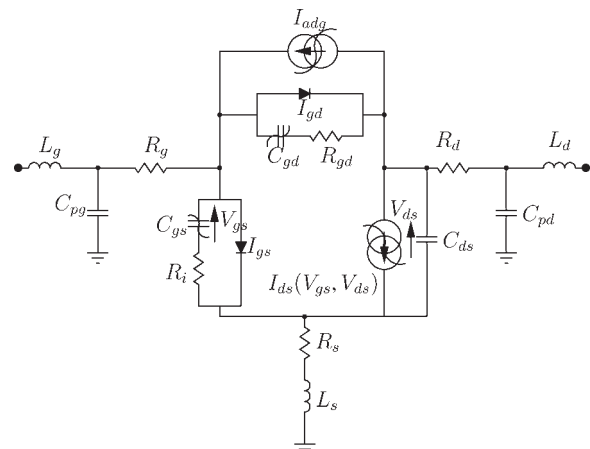

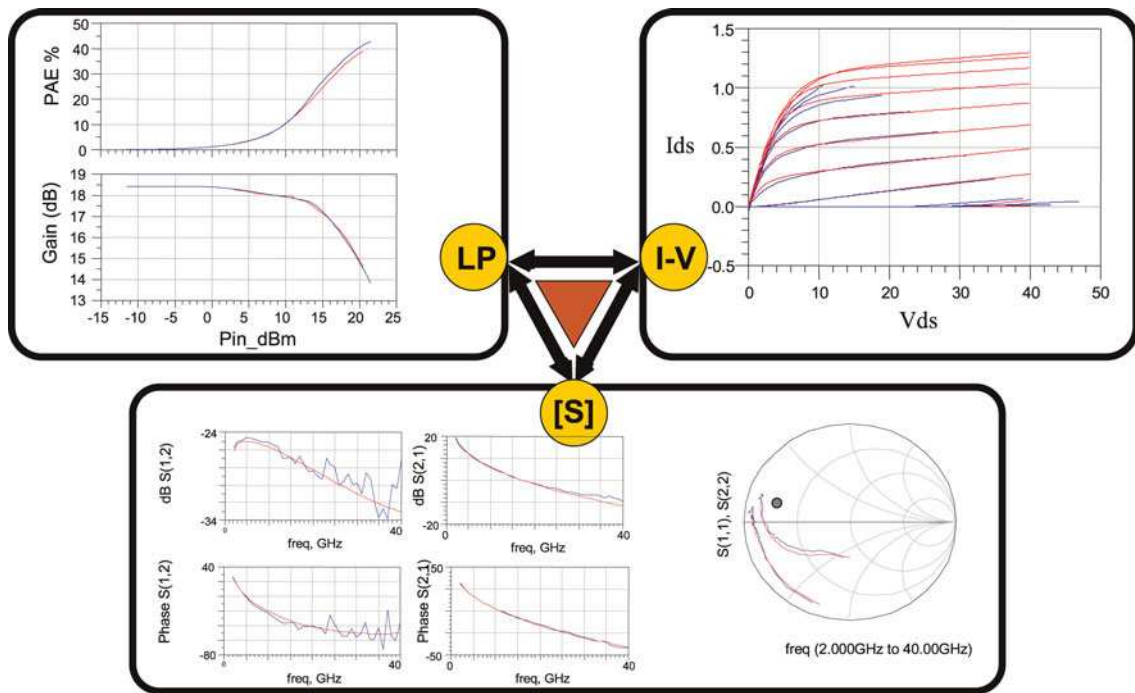**Fig. 4.** Nonlinear model of a GaN HEMT transistor in Agilent ADS.

Fig. 5. A validated nonlinear model released in the frame of KorriGaN. Every model is released with *I–V*, *S* parameters and load-pull measurements comparison.

the device self-heating. In fact, the device peak channel temperature is affected by power dissipation, and, due to the slow thermal dynamics, memory effects arise. Three-dimensional (3D) FEM-based thermal models are typically needed to account for the large-scale thermal dynamics related to the 3D nature of heat flow (influenced by the device geometry, layout, and multilayered structure, including heat spreaders and dissipators), and for the temperature dependence of the materials' thermal conductivity and specific heat, which makes the time-dependent heat diffusion equation nonlinear. On the other hand, due to the computational intensity of the 3D heat solver, the modeling of the nonlinear, dispersive thermal behavior at a system or circuit level calls for the

identification of compact models able to couple accuracy with numerical efficiency.

Within the KorriGaN project, Politechnico di Turino has developed a novel technique for the compact nonlinear dynamic thermal modeling of electron devices, based on the so-called behavioral Wiener approach. In the Wiener model, a nonlinear system with memory is approximated as the cascade of a linear system with memory and a nonlinear but memoryless system. The model can be readily extracted from 3D FEM simulations but also from thermal measurements as well; it allows for a simple and compact circuit implementation within the framework of available circuit simulators, and predicts with high accuracy self-heating dynamics over a wide range of input dissipated power levels and waveforms. Coupled with a temperature-dependent device nonlinear equivalent circuit, it allows for the thermal assessment of GaN-based power amplifiers, including the impact of thermal memory effects on the amplifier linearity [4, 5].

As an example of 3D FEM simulation, Fig. 7 (left) shows the mesh of a multifinger SELEX-SI GaN-HEMT (10 × 100 μm, only one-half of the device is considered) on top of a 70 μm SiC substrate. The substrated is glued to a Cu20W80 mounting through a 70-μm-thick layer of silver-filled epoxy resin (EPO-TEX H20E).

The temperature profile for a dissipated power of 4 W is shown in Fig. 7 (right).

Steady-state simulations at different power levels allow one to obtain the device thermal resistance shown in Fig. 8 (left). On the other hand, the dynamic thermal behavior may be extracted from the transient response to a small (linear case) input power step and transformed into the frequency domain, yielding the device frequency-dependent thermal impedance (Fig. 8 (right)). Following the Wiener behavioral approach, the large-signal (LS) compact model is then built-up as the cascade of the linear filter in Fig. 8 (right) and the nonlinear thermal resistance in Fig. 8 (left).
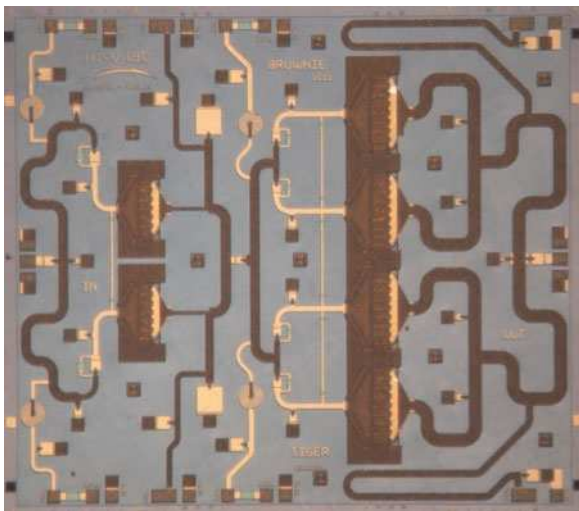

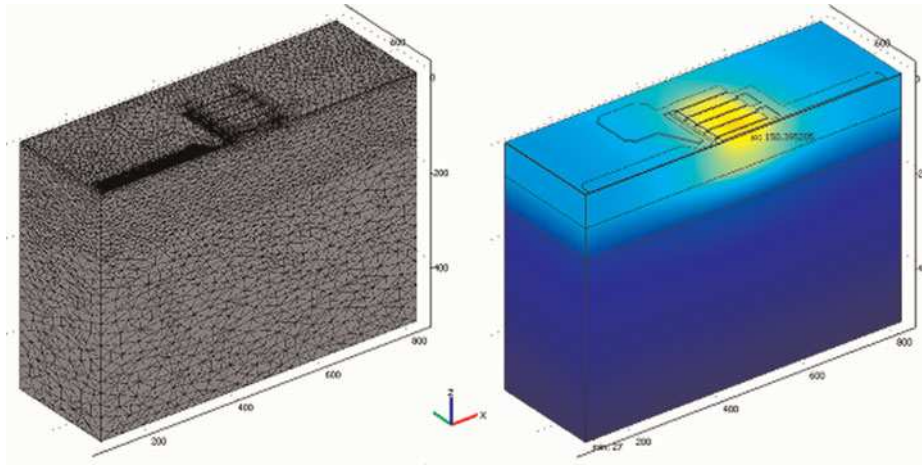**Fig. 6.** Photograph of amplifier. Chip size is 18 mm².

Fig. 7. Example of layout exploited for FEM simulations. One half of a SELEX-SI 10 × 100 μm AlGaN/GaN HEMT on 70 μm SiC substrate. (Left) Mesh discretization. (Right) Temperature profile at dissipated power of 4 W. Details on material thermal models can be found in [6].
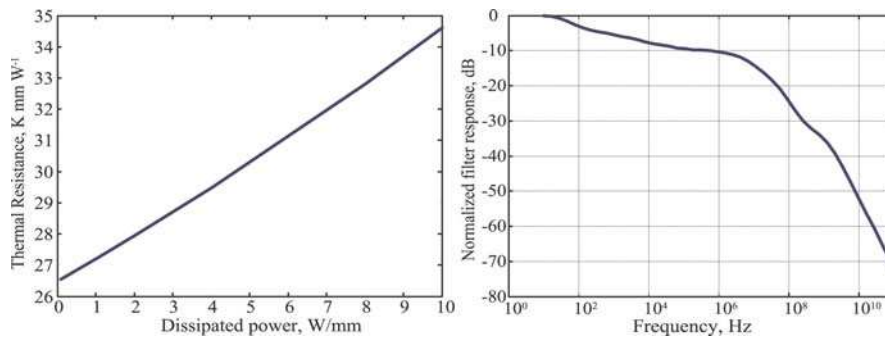

Fig. 8. Left: Thermal resistance of as a function of the dissipated power. Right: Normalized frequency response of the thermal impedance.

From a mathematical standpoint, such an approach corresponds to (a) applying an equivalent Kirchhoff transformation (see e.g. [7] and references therein) to the nonlinear time-dependent heat diffusion equation; (b) solving the resulting equation, which is still mildly nonlinear in the coefficient of the time derivative of the temperature, by approximating such a coefficient with a constant one. As a consequence, the Wiener model turns to be exact not only in the two limiting cases of T-independent material properties, or of steady-state behavior (zero time derivative), but also when the Kirchhoff transformation yields a transformed time-dependent heat equation that is exactly linear; this occurs when the materials' thermal diffusivity may be assumed as constant. Although this condition is not usually met in semiconductor devices, such remark provides a physical justification to the choice of the Wiener topology. The approach is validated against large-signal transient 3D thermal simulations in Fig. 9 for a wide range of dissipated power levels. The proposed model predicts with high accuracy the dynamic active region temperature increase, with a relative error limited to a few percent.
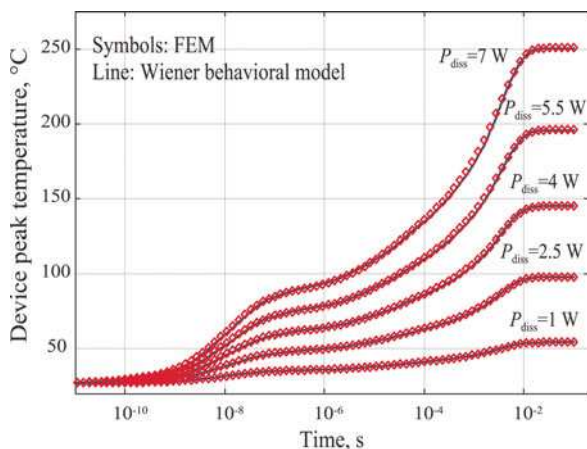
The Wiener thermal model was coupled to a temperature-dependent equivalent circuit electrical model according to the following strategy. From a physical standpoint, we can identify two main sources of temperature dependence in the device electrical behavior: the temperature sensitivity of the threshold voltage, the mobility and saturation velocity drop with increasing temperature. Temperature effects on reactive elements (such as capacitances) were found to be negligible in the considered frequency range and therefore not included in the model. To account for the afore-mentioned T-dependence, the drain current model coefficients connected to the threshold voltage were assigned a T-polynomial variation with respect to the value at the reference temperature, whereas an exponential dependence was given to the drain current variation related to the mobility decrease with temperature. Finally, a polynomial dependence was assigned to the parasitic resistances. The T-dependent model was then implemented as an
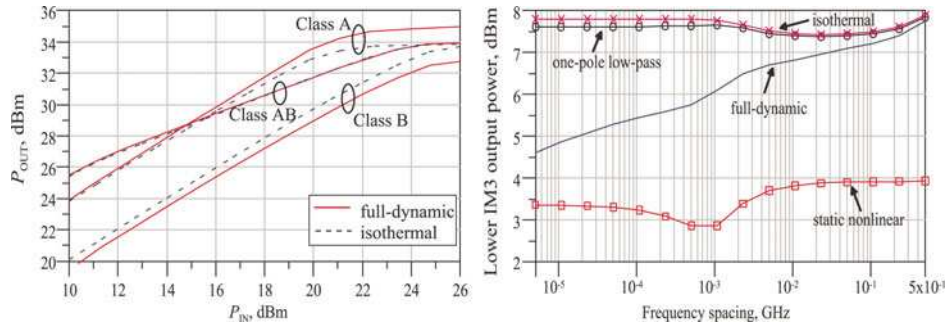

Fig. 9. Comparison between FEM solution and Wiener behavioral model.

Fig. 10. Left: Single tone simulation at 4 GHz on optimum power load (from [4]). Right: Two-tone simulation as a function of the tone spacing. The center frequency is 4 GHz, the total input power level is 25 dBm corresponding to 36 dBm output power (from [4]).

SDD Agilent ADS block, where the channel temperature is the voltage of an additional node connected to the compact thermal model, whose input current is evaluated as the instantaneous device dissipated power. The model is first fitted in the non-reactive part at a constant (reference) temperature through pulsed DC measurements; then, the reactive part is derived from S-parameter characterization. The temperature dependence is finally recovered by fitting to the static DC curves. A final refinement can be carried out by means of multibias S-parameter fitting.

The electrothermal self-consistent model can be used to gain insight into the impact of thermal effects on power amplifiers' linearity [4]. As an example, we study the impact of different thermal modeling choices on the prediction of the nonlinear performance of a 1 mm SELEX-SI coplanar GaN-based amplifier. In particular, we compare the full-dynamic thermal model previously presented to an isothermal one, in which the temperature is kept constant to the quiescent value. Fig. 10 (left) shows the simulated Pin–Pout curves on optimum loads under class A, class AB, and class B operation (4 GHz fundamental frequency). The isothermal model underestimates the output power under class A (since it neglects the device cooling due to the RF power under LS operation), while overestimates the output power at class B operation (device heating due to the RF power under LS operation); finally at class AB the two models give comparable results. As a further example, Fig. 10 (right) assesses the impact of electrothermal feedback on the third-order intermodulation product (IMP3) under two-tone excitation. Besides the full-dynamic and isothermal model, we consider also a single-pole low-pass model (cut-off frequency of 10 Hz) and a static nonlinear model. The change of electrothermal feedback (zero for the isothermal

model and increasing from single-pole, full-dynamic and static nonlinear models) causes a marked difference in the predicted IMP3 power and dependence on the tone spacing.

VI. TRAPPING EFFECTS

The modeling of the trapping effects was a research activity started thanks to the KorriGaN project [8].

To evaluate the influence of gate lag and drain lag we perform characterizations on every HEMT devices.

First of all, a cold bias point IV-network is performed. In this case, the quiescent bias point is $V_g = V_d = 0$ V. The instantaneous bias point is changed in order to trace the complete IV characterization. Therefore, the gate voltage is swept from pinch off to $V_g = +1$ or $+2$ V for complete drain voltage curves.

Then, we perform a GATE LAG network. The quiescent bias point is $V_g =$ pinch off and $V_d = 0$ V. The thermal behavior is very close to the cold network because there is no drain current. Thus, the difference between this IV-network and the cold one is the lag related to the gate voltage.

Finally, a DRAIN LAG + GATE LAG network is measured with a quiescent bias point as $V_g =$ pinch off and V_d on the final application value (25 V for example). There is no drain current for this bias point, so the thermal influence on the transistor is minimized. On the complete network, the difference between the GATE LAG and the DRAIN LAG + GATE LAG network is the drain lag effect.

Figure 11 illustrates gate and drain lag effects on pulsed IV measurements.

The detailed description of the nonlinear model including thermal and trapping effects is given in [8]. It allowed to describe
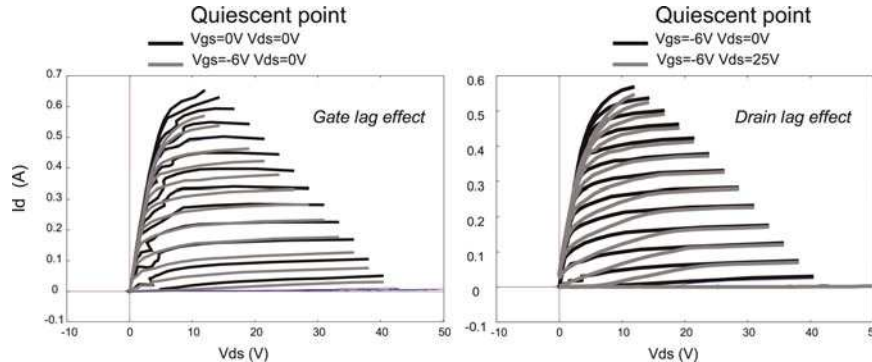

Fig. 11. GATE LAG (left) and DRAIN LAG + GATE LAG effects (right) on a QinetiQ 8×75 μm transistor.

accurately a lot of experimental phenomena exhibited during the pulsed *I–V* measurements as well as the RF power measurements.

For designers, the gate and drain lag models are sub-circuits located before the voltage command of the main current source. These sub-circuits include several "envelope detector". Each envelope detector has a filling time constant and a release one for trap. The principle is quite simple: basically, the detector modify, according to the RF level, the voltage command of the main current source. It means that the RF IV-network changes dynamically because of the traps. And the time constants, related to these traps are extracted from a pulsed measurement.

In most large-signal characterizations of KorriGaN HEMT, we can see that the DC current decrease versus the input power and then increase normally. This current slop phenomenon is due to trapping and its induced current degradation. It is taken into account by the trapping model (Fig. 12).

VII. NOISE MODELING

As it is well established, noise parameters of microwave FETs can be determined using two main approaches.

In the first one [9, 10], noise figure is measured by loading the device by a minimum of four source impedances synthesized by a tuner, and noise parameters are subsequently determined by a fitting procedure applied to the function expressing the dependence of the noise figure on source admittance. Nevertheless, to reduce the problems inherent to the measurements' uncertainties, more than four noise measurements are typically performed at each frequency. This approach has some drawbacks: apart from the cost and measurement bench complexity, the selection of the source admittances is limited by its losses; moreover, the measurement procedure is time-consuming, implying the preliminary or on-site linear characterization of the tuner; finally, the extracted noise parameters may not represent a physical device, since the selection of source admittance patterns critically affects the accuracy of the resulting noise parameters, resulting from a blind optimization.

In the second approach, the noise behavior of the intrinsic part of the active device is described by its small-signal equivalent circuit and some frequency-independent noise constants [11–14]. In particular, in [13] the noise of the active region of the device at microwave and higher frequencies is modeled utilizing equivalent thermal noise sources. The noise constants associated to the small-signal equivalent circuit of the device therefore
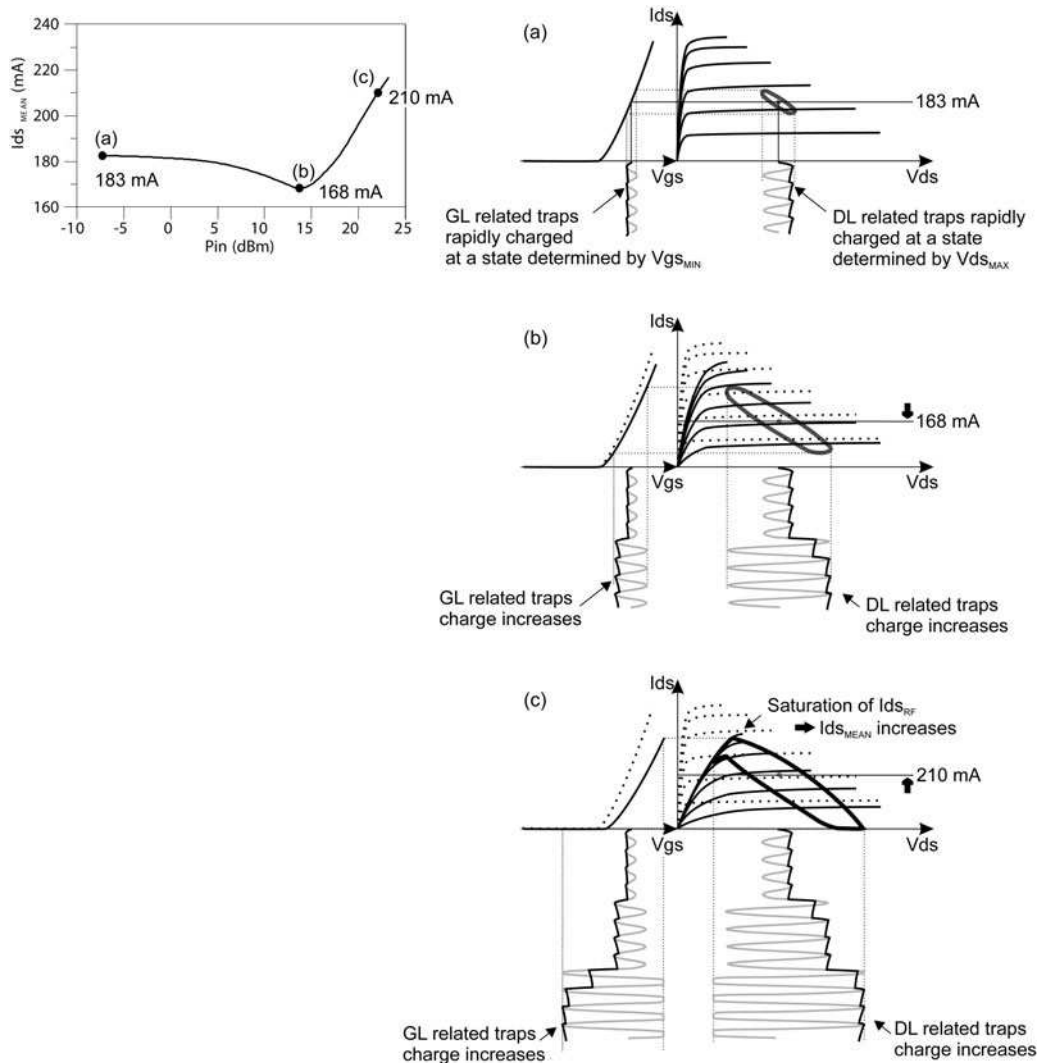

Fig. 12. Evolution of the drain current during a large signal characterization. This slope is taken into account by the model. On the IDS plot, gray line is the model without trapping effects, red line is the model including a trapping effect, and the crosses are the measurements.

typically consist in two frequency-independent equivalent noise temperatures assigned to the intrinsic gate and drain resistances. Such temperatures can be determined from the device noise figure corresponding to a matched source impedance (usually indicated by F50), measured at two different frequencies. Moreover, assuming the gate equivalent noise temperature to be equal to the ambient temperature [13, 14], a single F50 measurement at a given frequency is sufficient to determine the complete noise model. This approach does not require a tuner, resulting in a simpler test bench and in a straightforward noise measurement, if compared with the previous one. Moreover, the total number of measurements required for the determination of the noise parameters in a broad frequency range is remarkably reduced. On the other hand, a time-consuming determination of the small-signal equivalent circuit of the device is needed: the validity of the noise temperature model is strongly related to the validity of the equivalent circuit model.

During the project, however, a complete characterization is requested for active devices that are being realized, including small- and large-signal equivalent-circuit modeling. On this basis of such premises, the F50 method was considered the most efficient and straightforward. In fact, it allows one to share the small-signal equivalent circuit extraction step with large-signal modeling, further minimizing the number of the overall required noise measurements.

In detail, the considered noise model consists of the device small-signal equivalent circuit (depicted in Fig. 13) in which a noise source is associated to each resistive element (both intrinsic and extrinsic). Such noise sources represent the noise contribution of the device in terms of equivalent thermal noise.

The mean square value of each noise source is expressed via the respective physical resistance R_x and an equivalent noise temperature T_x; in particular, parasitic resistances are typically assumed to be at room temperature T_A. The following expressions therefore result:

$$\overline{e_{n,gs}^2} = 4kBT_{gs}R_i \tag{1}$$

$$\overline{i_{n,ds}^2} = 4kBT_{ds}G_{ds} \tag{2}$$

$$\overline{e_{n,G}^2} = 4kBT_A R_G \tag{3}$$

$$\overline{e_{n,S}^2} = 4kBT_A R_S \tag{4}$$

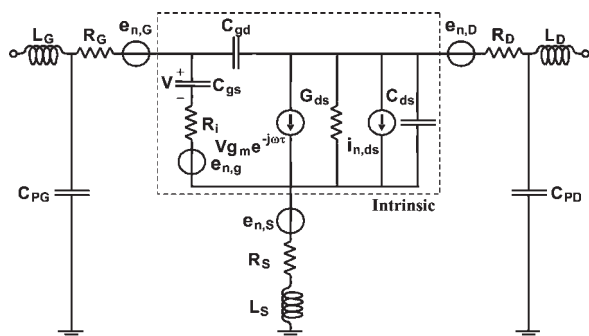$$\overline{e_{n,D}^2} = 4kBT_A R_D \tag{5}$$

Fig. 13. Small-signal and noise equivalent circuit model of the modeled GaN HEMTs.

where k is the Boltzmann constant and B is the frequency band.

The noise behavior of our GaN HEMTs is therefore completely characterized by the equivalent circuit of the device and the gate and drain equivalent noise temperatures (T_{gs} and T_{ds}, respectively) ascribed to the intrinsic gate resistance (R_i) and the drain-source conductance (G_{ds}), respectively. Such temperatures are constant with frequency: as a consequence, the frequency dependence of the device noise parameters is strictly related to the reactive elements of the equivalent circuit.

The model is therefore extracted in two steps: firstly, the equivalent circuit of the device is determined from S-parameters measurements; secondly, T_{gs} and T_{ds} are extracted making use of the equivalent circuit and F50 measurements.

S parameters of the GaN HEMTs under study have been measured in the 0.1–40 GHz frequency range in Cold-FET bias conditions (parasitics extraction) and for some bias points in the active region (intrinsic parameters). F50 measurements of the considered devices have been performed in the 2–18 GHz frequency range for all the previously selected bias points. Such measurements and the small-signal equivalent circuits have been utilized to determine the equivalent noise temperatures of the devices at the selected bias points. As a final step, the noise parameters of the devices have been computed utilizing the extracted equivalent noise temperatures and the small-signal equivalent circuits. In particular, the temperatures have been assumed to be frequency-independent, thus allowing the determination of the devices' noise parameters at frequencies higher than the measured ones.

Noise modeling was performed investigating the noise properties of nine GaN HEMT geometries, from two different foundries (Selex-SI and QinetiQ); in greater detail, the considered device peripheries from each foundry are 2×75 μm, 2×125 μm, and 4×125 μm from QinetiQ/Endeavour 0.25 μm coplanar foundry process; 2×50 μm and 8×75 μm from QinetiQ/Iona 0.25 μm coplanar foundry process; 2×50 μm, 4×50 μm, 4×75 μm, and 8×75 μm from Selex-SI 0.25 μm microstrip foundry process.

The models' extraction was carried out considering 20 and 30% (and in some cases 40%) of the I_{dss} current and at least two VDS voltage values (typically 10 and 20 V and in some cases 15 and 25 V).

As an example of the modeling activity, in the following two figures the four noise parameters, R_n, NF_{min}, and Γ_{opt} (amplitude and phase) for each GaN HEMT family are reported, considering a drain current equal to 20% of I_{dss} and 10 V of VDS for QinetiQ Endeavour and 15 V of VDS for Selex and QinetiQ Iona. Fig. 14 relates to Selex-SI while Fig. 15 relates to QinetiQ GaN HEMTs.

Due to the inherent higher breakdown voltage, GaN devices provide at least 20 dB higher survivability level when compared to GaAs pHEMTs [14, 15]. Use of GaN LNAs offers therefore interesting possibilities for simplified receiver front-end concepts, since an input protection limiter can be omitted, providing better overall system noise figure or better spurious-free dynamic range for increased sensitivity. Furthermore, the extracted 0.65 dB minimum noise figure exhibited by the characterized GaN technology at 10 GHz well compares with commercially available GaAs HEMT with comparable gate features.
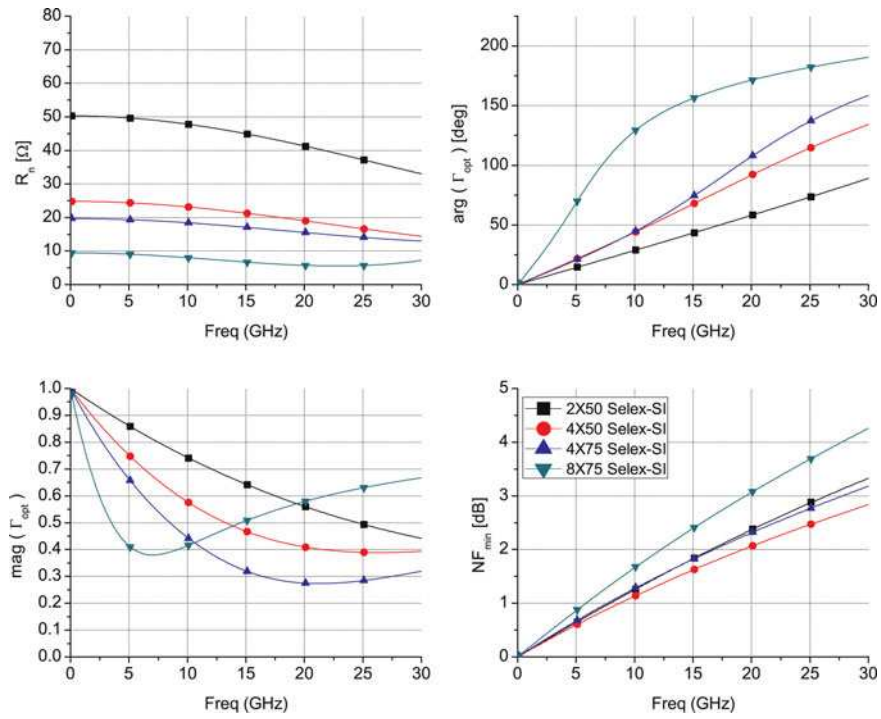
Fig. 14. Selex-SI GaN HEMTs noise parameters: R_n (top left), $\angle\Gamma_{opt}$ (top right), $|\Gamma_{opt}|$ (bottom left), NF_{min} (bottom right).
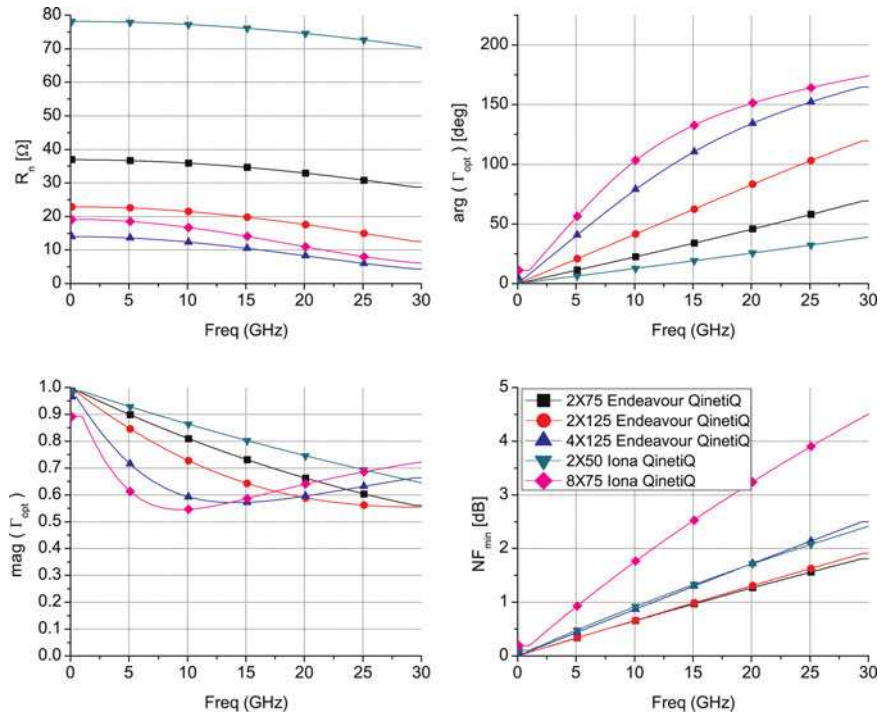

Fig. 15. QinetiQ GaN HEMTs noise parameters: R_n (top left), $\angle\Gamma_{opt}$ (top right), $|\Gamma_{opt}|$ (bottom left), NF_{min} (bottom right).

VIII. CONCLUSION

The modeling workpackage in KorriGaN has characterized and modeled every elementary cell (active and passive) of the project. Many characterizations were carried out: from classical [S] parameter measurements to large-signal characterizations in time domains.

The characterization of the KorriGaN transistors means for more than 100 measured transistors. The activities were uniformly distributed among the various partners.

In addition, a physical modeling aspect was developed simultaneously. European GaN technologies were optimized in that way. The project provided several validations of assumptions made during the equivalent circuit modeling of KorriGaN HEMTs (regarding the temperature).

One of the main advances in the modeling activity was the creation of new electro-thermal models and the trapping effect models.

A large number of models have been produced during the project: linear models, nonlinear models, noise models, electro-thermal models, and even trapping effect models to take into account the gate and drain lag. This project, including different institutes or technology centers, provides state of the art skills. This collaboration between various European partners has helped the raise of the European GaN technology at a non-negligible level within four years.

ACKNOWLEDGEMENTS

REFERENCES

[1] Gauthier, G.; Mancuso, Y.; Murgadella, F.: KORRIGAN – a comprehensive initiative for GaN HEMT technology in Europe, in *Gallium Arsenide and Other Semiconductor Application Symposium*, 2005, 361–363.

[2] Teyssier, J.-P.; Bouysse, P.; Ouarch, Z.; Barataud, D.; Peyretaillade, T.; Quere, R.: 40-GHz/150-ns versatile pulsed measurement system for microwave transistor isothermal characterization. IEEE Trans. Microwave Theory Tech., **46** (12) (1998), 2043–2052. doi: 10.1109/22.739281.

[3] Piotrowicz, S.; et al.: State of the art 58W, 38% PAE X-Band AlGaN/GaN HEMTs microstrip MMIC amplifiers, in *Compound Semiconductor Integrated Circuits Symposium 2008*, 2008. doi: 10.1109/CSICS.2008.39.

[4] Camarchia, V.; Cappelluti, F.; Pirola, M.; Guerrieri, S.D.; Ghione, G.: Self-consistent electrothermal modeling of Class A, AB, and B power GaN HEMTs under modulated RF excitation. IEEE Trans. Microwave Theory Tech., **55** (9) (2007), 1824–1831. doi:10.1109/TMTT.2007.903839

[5] Bonani, F.; Camarchia, V.; Cappelluti, F.; Guerrieri, S.; Ghione, G.; Pirola, M.: When self-consistency makes a difference. IEEE Microwave Mag., **9** (5) (2008), 81–89. doi:10.1109/MMM.2008.927638

[6] Cappelluti, F.; Furno, M.; Angelini, A.; Bonani, F.; Pirola, M.; Ghione, G.: On the substrate thermal optimization in SiC-based backside-mounted high-power GaN FETs. IEEE Trans. Electron Dev., **54** (7) (2007), 1744–1752. doi: 10.1109/TED.2007.899380

[7] Joyce, W.: Thermal resistance of heat sinks with temperature dependent conductivity. Solid-State Electron., **18** (4) (1975), 321–322. doi: 10.1016/0038-1101(75)90085-4

[8] Jardel, O.; et al.: An electrothermal model for AlGaN/GaN power HEMTs including trapping effects to improve large-signal simulation results on high VSWR. IEEE Trans. Microwave Theory Tech., **55** (12) (2007), 2660–2662. doi: 10.1109/TMTT.2007.907141

[9] Lane, R.Q.: The determination of device noise parameters. Proc. IEEE, **57** (8) (1969), 1461–1462.

[10] Pucel, R.A.; Haus, H.A.; Statz, H.: Signal and noise properties of GaAs microwave FET. Adv. Electron. Electron Phys., **38** (1975), 195–265.

[11] Gupta, M.S.; Greiling, P.T.: Microwave noise characterisation of GaAs MESFET's: determination of extrinsic noise parameters. IEEE Trans. Microwave Theory Tech., **36** (4) (1988), 745–751. doi: 10.1109/22.3580.

[12] Pospieszalski, M.W.: Modelling of noise parameters of MESFET's and MODFET's and their frequency and temperature dependence. IEEE Trans. Microwave Theory Tech., **37** (9) (1989), 1340–1350. doi: 10.1109/22.32217.

[13] Tasker, P.J.; Reinert, W.; Hughes, B.; Braunstein, J.; Schlechtweg, M.: Transistor noise parameter extraction using a 50 Ω measurement system, in *IEEE MTT-S International Microwave Symposium Digest*, 1993, 1251–1254. doi: 10.1109/MWSYM.1993.277100.

[14] Krausse, D.; et al.: Robust GaN HEMT low-noise amplifier MMICs for X-Band applications, in *Gallium Arsenide Applications Symposium*, 2004, 71–74.

[15] Micovic, M.; et al.: GaN MMIC technology for microwave and millimeter-wave applications, in *Compound Semiconductor Integrated Circuit Symposium, 2005. CSIC '05. IEEE*, 2005. doi: 10.1109/CSICS.2005.1531801.

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