Efficiency enhancement of GaN power amplifiers over a wide bandwidth by an active control of gate source voltage waveforms

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INTRODUCTION

This paper presents a technique to improve the power added efficiency (PAE) of GaN power amplifiers by an appropriate shaping of the gate source voltage waveform.

High efficiency performances of microwave power amplifiers are reached by implementing proper matching conditions at harmonic components.

For microwave applications, harmonic tuned amplifiers offer for the moment the best energy conversion efficiency between DC supply and RF power at fundamental frequency available in a 50Ω load.[1]

In addition to proper harmonic terminations, the minimization of power losses at fundamental frequency in the output RF matching and power combining circuit is of prime importance. This has been widely reported over the past few years. Considering this main aspect GaN technology offers an evident advantage due to its high drain voltage operation capability that is beneficial for designing low loss and wideband output matching circuits. Several works have been reported during the past few years.[2],[3],[4],[5],[6]

A problem encountered when designing high efficiency power amplifiers is to avoid getting high efficiency performances restricted to only a narrow frequency bandwidth around center frequency. It can be often observed that the higher the PAE is at center frequency, the quicker the PAE decreases at offset frequencies each side away from the center frequency. This can be attributed to high Q resonant tuning conditions.

We point out and examine in this paper a major role played by the gate source voltage waveform in PAE performances over a frequency bandwidth of interest.

For power amplifiers operating at saturated power, a significant second harmonic current component exists at the gate port and is terminated into a passive resonant circuit like for example a quarter wave length line used in the gate bias circuit. For offset frequencies, phase conditions of the passive source impedance at second harmonic vary and lead to non appropriate enlarged gate source voltage waveform upper the pinch off value.

That leads to larger turn on time of the drain current resulting in a larger overlapping between drain current and drain voltage prejudicial for dissipated power and power added efficiency.

In this paper we present a solution to maintain an appropriate gate source voltage shape.

It consists in driving the gate of a power stage with an appropriate half sine voltage shape supplied by a driver stage operating at low drain bias voltage.

GATE SOURCE VOLTAGE SHAPING:

For high efficiency conditions, the device is driven at significant gain compression. A significant amount of second harmonic component generated by the transistor flows into the source network.

Harmonic 2 plays a major role and must be properly controlled by the source network. Otherwise the intrinsic gate source voltage can be distorted, the worst case being an "inverse" half sine wave shape that results in a significant increase of the DC drain current and a decrease of PAE performances. This worst case condition leads to an increase of the ON time "t_{ON}" and consequently a wider "aperture angle" of the transistor.

On the contrary, if an appropriate control of the input gate source voltage shape is achieved to reach an half sine wave shape, the on time t_{ON} and the aperture angle are reduced. It results in a reduction of the DC drain current along with a minimization of the drain voltage and drain current overlapping [2] [3].

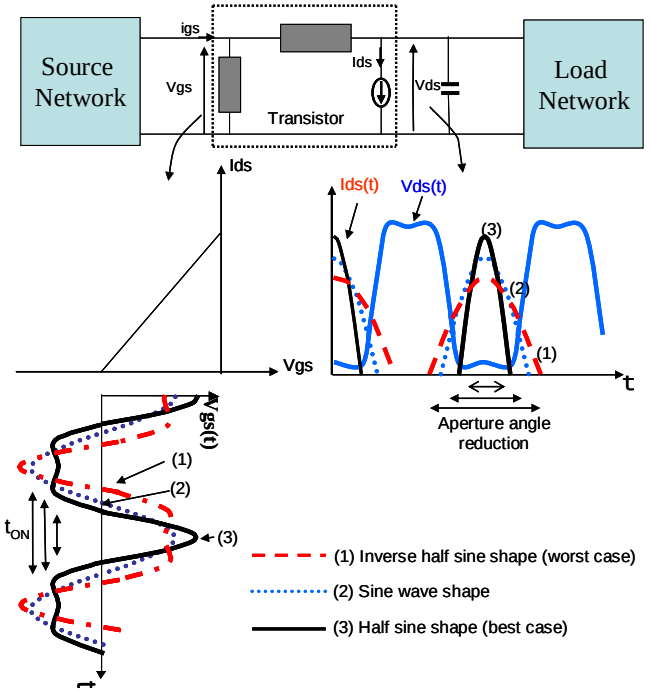

Fig. 1. Illustration of the effect of the input voltage shape on the aperture angle.

Best and worst case conditions are sketched in Fig. 1 in the case of a class F operation mode.

The theoretical half sine wave gate source voltage derived from analytical Fourier series expansion limited to two harmonics is:

$$Vgs(t) = V_{gs0} + V_{gs1} * \cos(wt) + V_{gs2} * \cos(2 * wt + \phi)$$

Optimum waveform shaping is obtained for Vgs2=Vgs1/7 and φ=0 as illustrated in Fig. 1 (case 3).

An experimental validation by using high impedance probes and large signal network analyzer measurements has been reported in [7].

The following focuses on the design of a two stage PA including a driver stage that drives the power stage input with an appropriate voltage waveform.

SIMULATION RESULTS

The two stage PA has been design by using 15 W GaN die from CREE. A nonlinear model has been extracted using pulsed I/V and pulsed S parameter measurements.

The following study was performed at the transistor bias point V_{gso2}=- 2.3V and V_{dso2}=28V for the power stage and V_{gso1}=-2.0, V_{dso1}=7V for the driver stage. The operating center frequency is 2 GHz.

HB simulations using ADS package have been carried out using ADS package The design topology is shown in Fig 2.

The output power stage operates under class F conditions. Harmonic load impedances are tuned to: Z_{L1}=37-j2 Ω at Fo; a low impedance Z_{L2} close to a short at 2Fo and a high impedance Z_{L3} close to an open at 3Fo.

To feed the power stage input with a quasi half sine shape voltage, we use a driver stage that operates in an inverse class F operation mode.

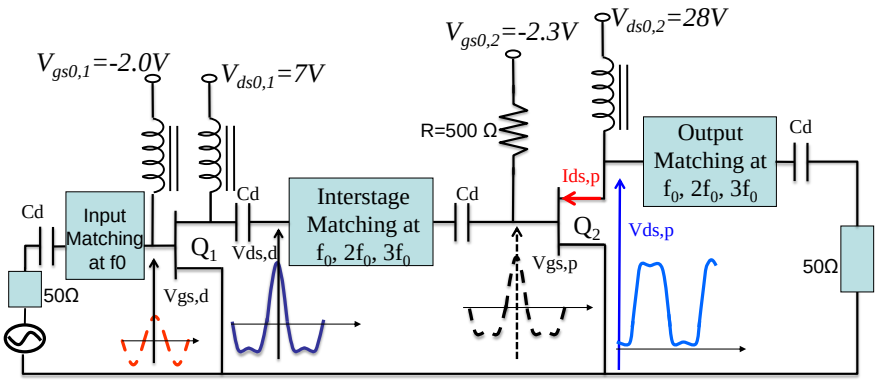

Fig. 2 Two stage amplifier topology.

The inter stage matching network is designed to meet two requirements:

First, a proper power matching at the fundamental frequency.

Second, a proper control of the voltage transmission factor at harmonic 2 in order to target a half sine shape voltage at the gate port of the power stage.

Figure 3 shows simulation results of the two stage power amplifier. 70% PAE is obtained at 2GHz with 42dBm of output power and 29dB power gain.

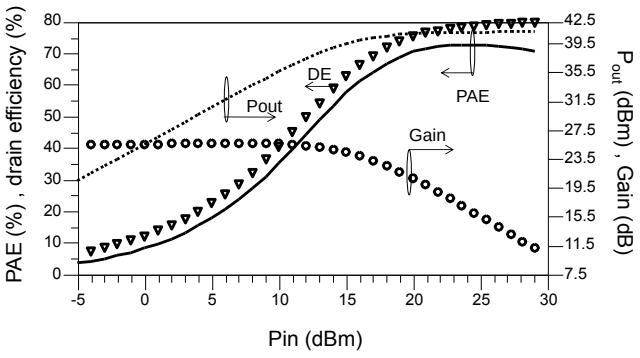

Fig. 3 simulation results of two stage amplifier at 2GHz

CIRCUIT DESIGN and MEASUREMENT RESULTS

In order to demonstrate the benefit provided by this approach, a two stage PA and a single stage PA having the same output power stage have been built on alumina substrate. A photograph of the built-in amplifiers is shown in figure 4.

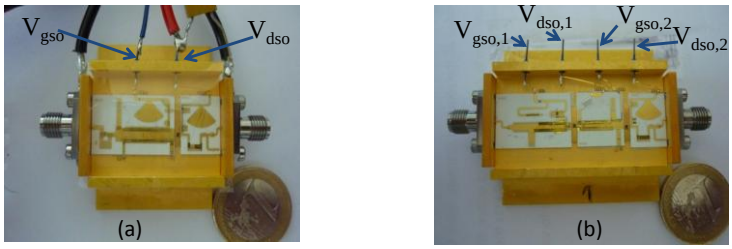

Fig. 4 Built-in power amplifiers: single stage (a) and two stage (b) .

The output matching circuits at fundamental and harmonics of the two amplifiers are rigorously the same. For the single stage PA, second harmonic termination at the input is achieved by the quarter wavelength line used for

gate biasing. For the two stage power amplifier, an active second harmonic injection at the input of the power stage is performed thanks to the driver stage.

Figure 5 shows power and efficiency measurements of the two amplifiers versus frequency.

The design of the two stage PA offers 4 point PAE improvement at center frequency 2GHz associated to 8dB gain increase compared to the power stage alone without affecting output power performances (Pout=41.8dBm). The main benefit of the proposed design is to get good PAE performances over a wider frequency bandwidth.

At 2.2 GHz, the two stage power amplifier offers 10 point of PAE enhancement.

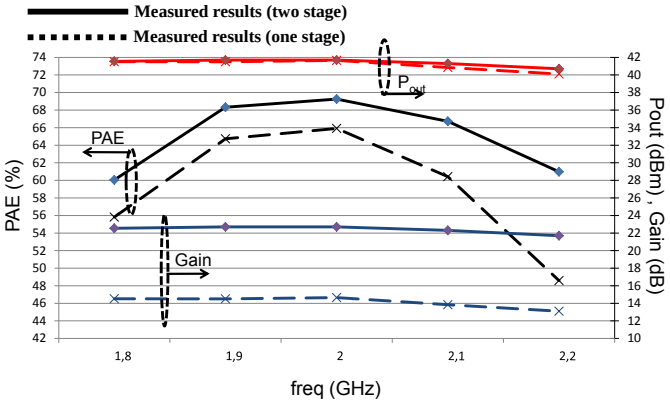

Fig. 5 Measurement results of two power amplifiers at 4 dB gain compression.

CONCLUSION

This paper has highlighted the prime importance of an appropriate gate-source voltage waveform control for the design of high efficiency GAN amplifier. A design method of a two stage power amplifier has been reported. The two stage PA includes a driver stage to control appropriate second harmonic component injection at the gate port of the power stage. This principle mainly reveals to be valuable to extend PAE versus bandwidth performances.

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