New compact power cells for Ku band applications

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***Abstract*—This paper reports on the design of new power cells based on GaAs PHEMT transistors with 0.25µm gate length in MMIC technology. The design starts from a fishbone power cell initially designed by United Monolithic Semiconductors (UMS). This one allows us to validate the elementary transistor model. This model is used for other power cells design as cascode cell.**

Keywords-component; compact; cascode cell; power amplifier; MMIC; PHEMT; Ku-band

I. INTRODUCTION

The important demand of power amplifiers with high performances and low cost requires the development of chips more and more compact [1] [2]. In order to increase the compactness of these devices, we can, for instance, decrease the size of its power cells. In the 2W amplifier performed by the UMS foundry[3], the size of this amplifier was decreased thanks to this method. In this article, the power cell used in the 2W amplifier of UMS, allows us to validate an elementary transistor model with two gate fingers. This model represents the building block to design other innovative power cells.

II. VALIDATION OF TRANSISTOR MODEL USED IN THE POWER CELL

A. Fishbone cell structure

The new last stage power cells of the power amplifier marketed by UMS, is composed of four transistors of 1.2 mm gate width each. In order to have a more compact chip, transistors have been replaced by two power cells called fishbone.

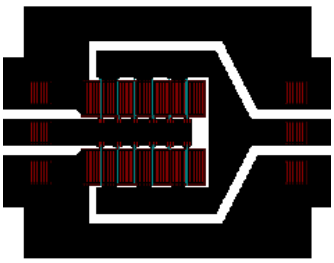

Figure 1: Layout of a fishbone structure

Each cell relies on two GaAs PHEMT transistors of the UMS foundry with twelve gate fingers of 100 µm width and 0.25 µm length. There are via holes in the source of transistor. The device is much smaller than a single 24x100 µm transistor because gate bus and drain bus are no longer vertically distributed but they are horizontally distributed (Figure 1)

[S] parameters measurements from 2 to 40 GHz as well as load pull measurements between 10 and 16 GHz of power cell with 3 mm of gate development, have been realized for a bias point V_D=8V, I_D=130mA. Initial measurements and simulations results were not in a good agreement in the whole frequency band. So, the 12x100 µm global model of transistor was not sufficient to describe the power cell performances.

B. Validation of the transistor model with two gate fingers

In order to improve the model precision of the power cell, a new approach to simulate the basic cell has been defined. The shape of basic cell composed of the two PHEMT facing each other and perpendicular to the signal propagation, encourages the use of a distributed approach. In fact, the 12x125 µm model is divided in several smaller size models. To simplify the power cell model, the smaller size model of PHEMT is defined as a 2x125 µm model. Parameters are scaled from those of the 12x125 µm transistor.

In Figure 2, pulsed scattering parameters measurements have been performed by UMS and compared to simulations from 2 to 40 GHz. There is a good agreement between measurements and simulations. This involves truthfulness of power cell model and therefore, the truthfulness of the two gate fingers transistor model used.

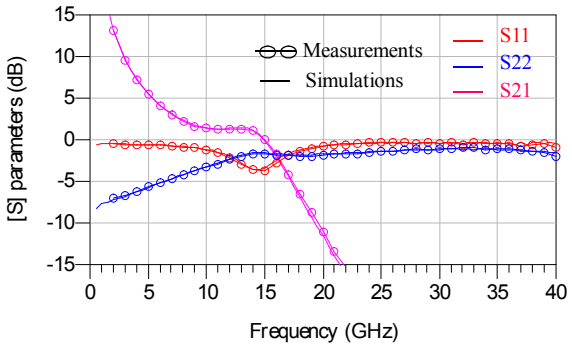

Figure 2 : Comparison between measured and simulated S parameters of the fishbone cell

Load pull measurements have been also performed in order to verify and compare optimum power results with simulation results. Figure 3 shows the gain and the output power results obtained at 10 GHz. The power added efficiency is shown Figure 4.

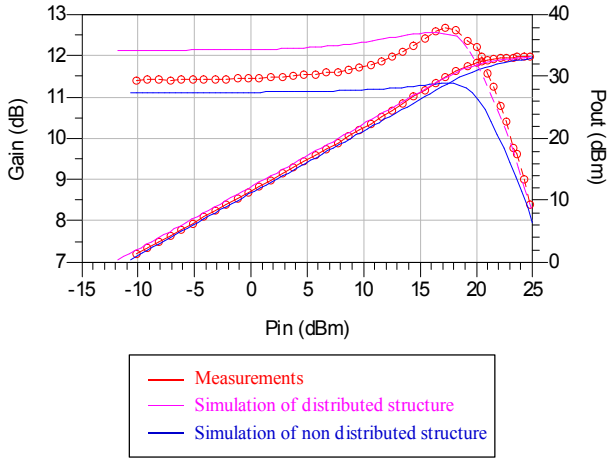

Figure 3 : Comparison between simulations and measurements of the gain and output power at 10 GHz

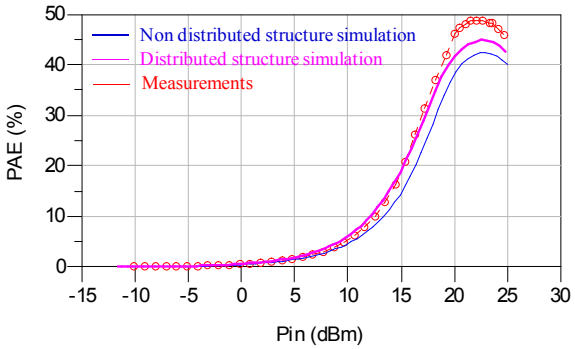

Figure 4 : Comparison between PAE simulations and load pull measurements at 10 GHz

III. PRINCIPE OF INNOVATIVE CASCODE CELL DESIGN

Thanks to this transistor model with two gate fingers, we can design other very compact power cells. We have chosen to design several kinds of cascode cells [4] [5] [6]. Indeed, these one are more compact than a single transistor with the same gate development, or than a fishbone cell. They have a higher gain and a better output impedance. The input/output isolation is also really improved.

The cascode cell is made up of two transistors in cascade. The first one is in a common source configuration. Its drain is connected to the source of the second transistor which is in a common gate configuration. A Ca_1 capacitance as shown in Figure 5 is added to the gate of the second transistor in order to create a voltage divider bridge. This one avoids that the total drain voltage variation of the first transistor is applied to the input of the second. The theoretical formula is the following:

$$Ca_1 = \frac{Cgs}{\left(\left|\frac{Vds_1}{Vgs_2}\right| - 1\right)}$$

This capacitance is optimized for power applications.

Cascode cell being sensitive to oscillations, a study of linear stability must be realized with optimization of the Ca_1 capacitance. To avoid all instability phenomenons, a resistance is added in series with the Ca_1 capacitance. It allows to ensure the stability but unfortunately power performances are damaged. Then, we must perform both the optimization of these two parameters and a new output matching of the cell.

IV. CASCODE CELL STRUCTURE

Thanks to the validation of the transistor model with two gate fingers, we have designed several cascode cells. The two 12x100 µm transistors used for these cells are distributed with six 2x100 µm transistors. Each device has been designed thanks to CADENCE software. The first design inserts the Ca_1 capacitance and the stability resistance between each transistor of the distributed structure presented in Figure 5. This topology increases significantly the compactness of the cell.

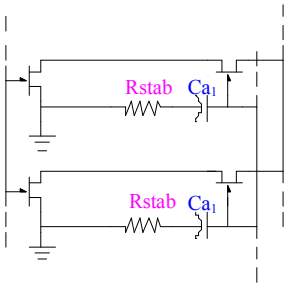

Figure 5 : First structure of PHEMT GaAs cascode (called CAPA IN)

The second topology inserts the Ca_1 capacitance and the stability resistance outside of the cell as shown in Figure 6.

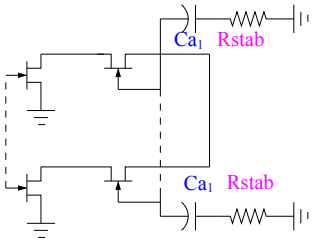

Figure 6 : Second structure of PHEMT GaAs cascode (called 2 CAPAS)

The UMS foundry has not given us the authorization to show the layout of these new cascode cells. That is why, we only show the principle schematic of these structures. Below, an overview table of dimensions for the different devices.

TABLE I. Size of each cell

	24x100 µm	**Fishbone**	**Cascode version1**	**Cascode version2**
Vertical size(µm)	780	710	412	549

V. SIMULATION AND MEASUREMENT RESULTS

First, the passive parts have been simulated on electromagnetic software MOMENTUM. [S]parameter simulations and measurements from 0.5 to 40 GHz have been performed for each cascode cell topology. The bias point is V_D=16V and I_D=150mA. During measurements, the biases order is very important because if there is a mistake in the bias order, this can involve the cascode breakdown. We have observed the results obtained on the gain, the input/output isolation and on the output impedance. In fact, we have studied the three main advantages of cascode cell. Figure 7 shows the simulated and measured small signal gain of cascode cells. Cascode cell gain is better than common source transistor gain until 23 GHz. We recall that measurements are good from 0.5 to 26 GHz because the bias tees do not operate above this frequency. We have a good agreement between simulations and measurements.

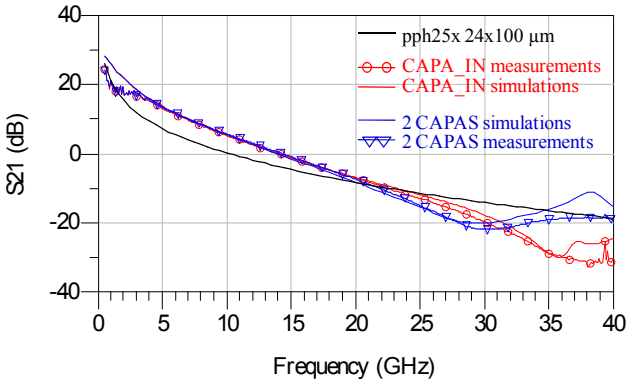

Figure 7 : Linear simulations and S21 measurements of each cascode structures compared to a common source transistor with the same gate development

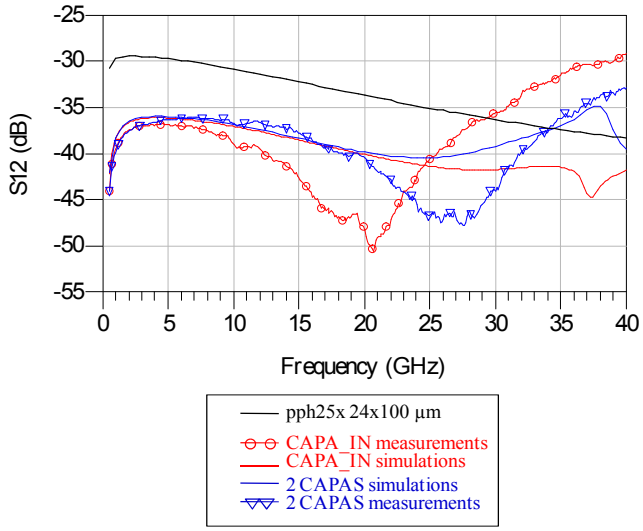

Figure 8 : Linear simulations and S12 measurements of each cascode structures compared to a single transistor with the same gate development

The input/output isolation is shown Figure 8. For cascode cells, the input/output isolation is better than a single transistor. However, for the two cascode cell topologies, a difference between simulation results and measurements has been obtained. Transistor model used during simulations is an existent model, thus, this can explain the differences between simulations and measurements. An adjustment of model parameters need to be performed.

The Figure 9 shows output impedances simulations and measurements for the two topologies studied. These results are compared to a single transistor with the same gate development. Simulations results are agree with measurements performed and the output impedance of cascode cell is bigger than a single transistor that is consistent to the theory.

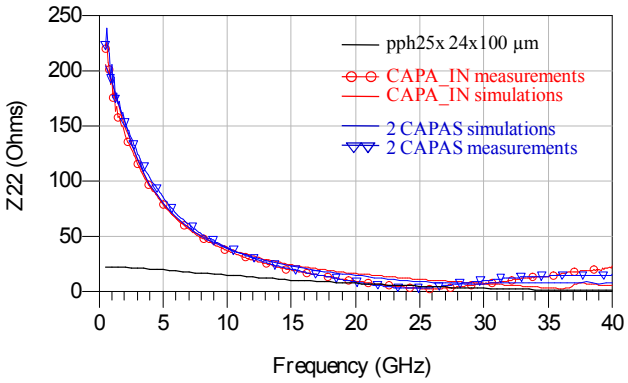

Figure 9 : Linear simulations and Z22 measurements of each cascode structures compared to a single transistor with the same gate development

In order to have a complete linear study, we have performed a first approach for the stability analysis of each structure. Figure 10 shows the Rollet K factor and the determinant of S matrix, delta.

The Rollet K factor shows that each topology studied is not unconditionally stable on the whole frequency band. The study of stability circles must be realized in order to know if the cascode cell is stable or not on the studied frequency range. Thanks to this study, we have shown that these two cascode cells are linearly stable on the whole frequency range.

A proof of linear stability is that during [S] parameter measurements, no oscillation appeared.

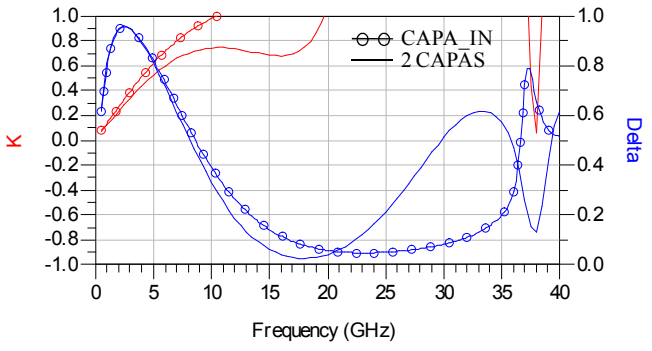

Figure 10 : Rollet factor and determinant of S parameter matrix of each cascode structure from 0.5 to 40 GHz

Load pull simulations on each topology were performed from 10 to 16 GHz. Load pull measurements are in progress and might be available for the conference day. The Figure 11 shows the maximal PAE obtained of each cascode cell. It reaches 43 % whereas for a common source transistor it reaches nearly 60 %.

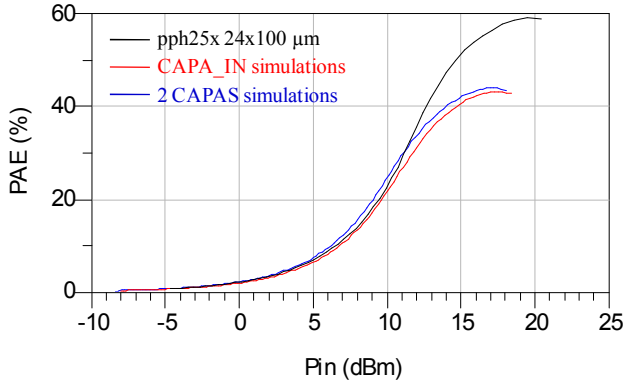

Figure 11 : Cascode cells PAE compared to a single transistor PAE at 10 GHz

The main advantages of these cells are that power gain increases (Figure 12) and meanly the output power (Figure 13) which is the same or bigger than a single transistor with the same gate development. So, cascode cell exhibits a better power density.

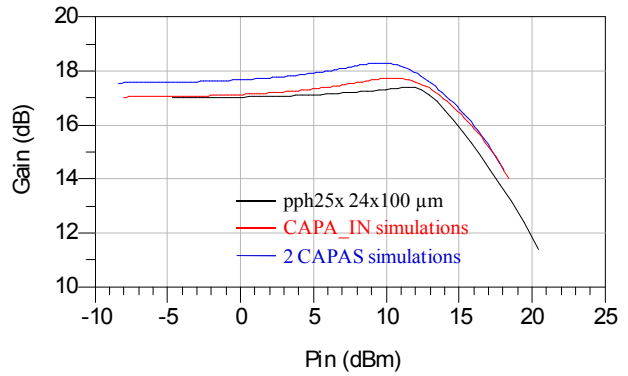

Figure 12 : Power gain of each cascode cell compared to a single transistor with the same gate development at 10 GHz

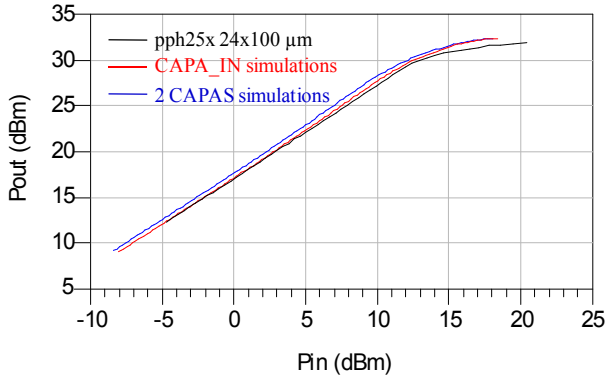

Figure 13 : Comparison between output power of cascode cell and a single transistor at 10 GHz

VI. CONCLUSION

New very compact power cells with GaAs PHEMT transistor have been designed with UMS MMIC technology. The fishbone power cell has allowed us to validate the elementary transistor model with two gate fingers. Thereafter, this transistor has enabled us to design other compact power cells based on the cascode topology. The comparison between these new cells and a single transistor exhibits a better gain for the cascode cell, an output power equivalent and power added efficiency equal to 43 % at 10 GHz.

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